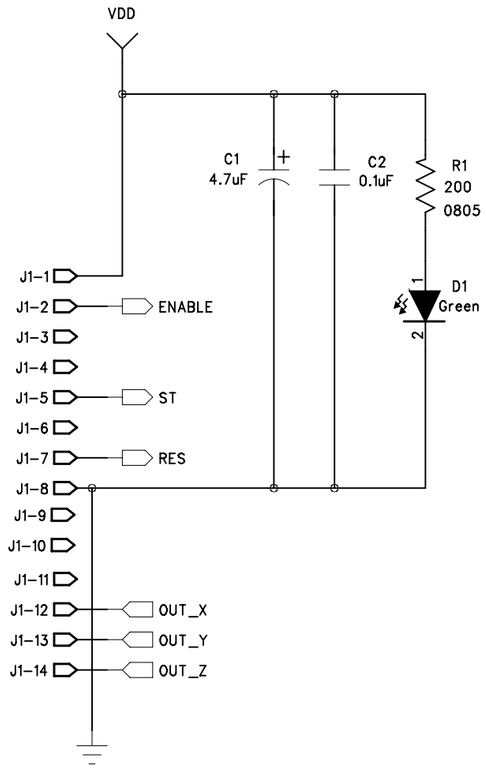

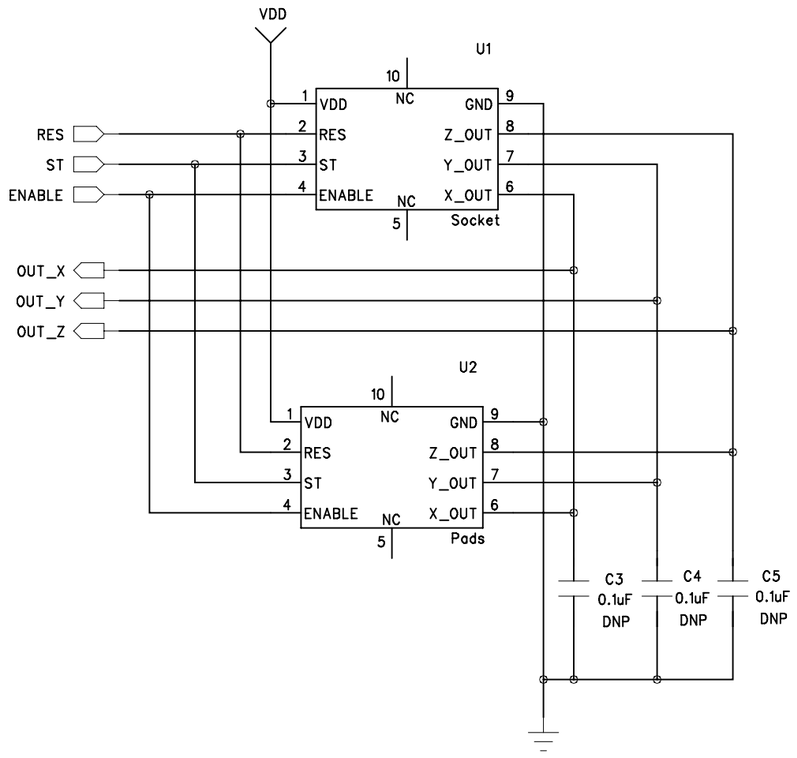

PIN	KXCT9	KX220		
1	VDD	VDD		
2	RES*	RES*		
3	ST**	ST**		
4	ENABLE***	ENABLE***		
5	NC	NC		
6	X Output	X Output		
7	Y Output	Y Output		
8	Z Output	Z Output		
9	GND	GND		
10	NC	NC		

*RES pin 2 is reserved and should be tied to VDD or GND.
**ST pin 3 is for self-test and should be tied to GND for normal operation.
***ENABLE pin 4 should be tied to VDD for normal operation.

NOTES:

1) All resistors are 1%, 1/10W, 0603 unless otherwise specified.
2) All ceramic capacitors are 10%, 50V, 0603, X7R unless otherwise specified.
3) U1 socket: Loranger International, 03717 111 6218A.

DRAWN: J Zappala	DATED: 03/08/2017
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

COMPANY: Kionix Inc.

TITLE: KXTC9 Evaluation Board

DRAWING	SIZE:	DRAWING NO:	REV:
DWG677	B	KAMMDM001R41	1

SCALE: None. SHEET: 1 OF 2

REVISION RECORD				
DATE:	DRAWN BY:	DESCRIPTION:	CHECKED BY:	DATE:
03/01/2010	B Ross	1) Initial release.		
03/08/2017	J Zappala	1) Add: table for pin-out, Notes, DNP to C3, C4, and C5.		
		2) Update device pin-out and net names to current specifications.		

MTHOLE1
MTHOLE120

MTHOLE2
MTHOLE120

MTHOLE3
MTHOLE120

MTHOLE4
MTHOLE120

DRAWN: J Zappala	DATED: 03/08/2017		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		

COMPANY: Kionix Inc.

TITLE: KXTC9 Evaluation Board

CODE:	SIZE:	DRAWING NO:	REV:
DWG677	B	KAMMDM001R41	1

SCALE: None.

SHEET: 2 OF 2