Introduction

This technical note is intended to provide information about the proper RESET of the Kionix KXR94, and KXD94 accelerometers.

Power-On Reset

Proper functioning of power-on reset (POR) is dependent on the specific **Voff** and **Toff** profile of individual applications. It is recommended to minimize **Voff** and maximize **Toff**. To assure proper POR in all environmental conditions the application should be evaluated over the range of **Voff**, **Toff** and temperature as POR performance can vary depending on these parameters. It is also advised that the Vdd ramp up / ramp down be monotonic. Note that the outputs will not be stable until Vdd has reached its final value.

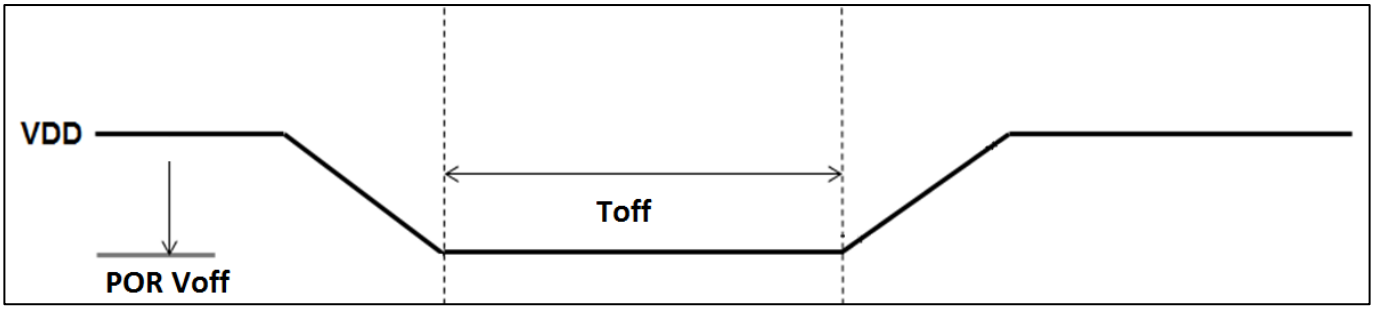

Figure 1. POR Voff and Toff Timing Diagram

36 Thornwood Drive, Ithaca, NY 14850 USA
Tel: 607-257-1080 — Fax: 607-257-1146
www.kionix.com — info@kionix.com

Example POR Performance

As an example, testing was performed on a particular setup to determine the conditions required to assure proper POR. The power supply to Vdd had to be held to within the regions indicated in Figure 2 below. Note how the **Voff** and **Toff** conditions for proper POR vary with temperature. In this example, testing at -40°C showed the power supply voltage (**Voff**) had to be held below the POR Threshold of 0.03 Volts for more time than 500 ms (**Toff**) to assure that POR was properly executed.

The user may wish to establish an operational range as shown in the chart below:

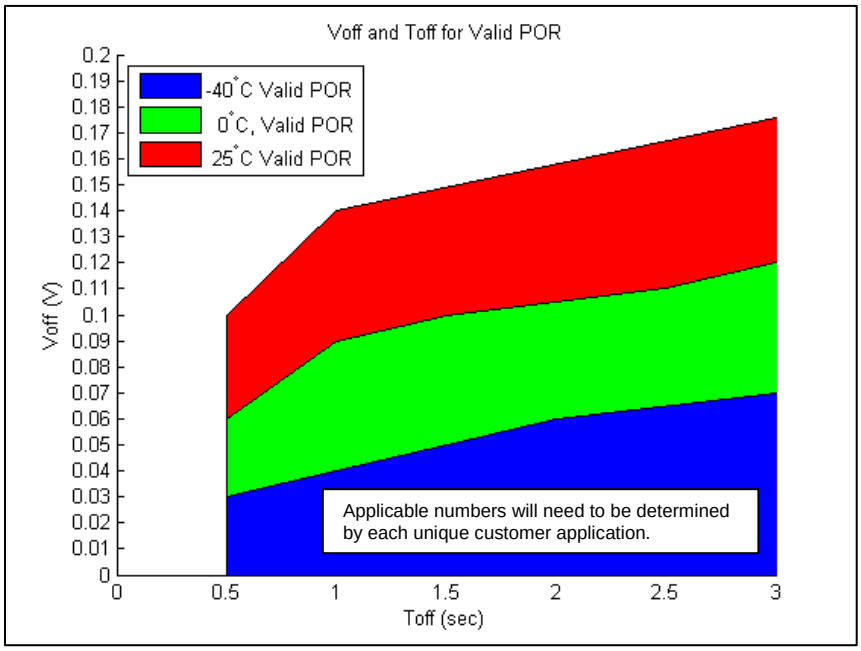

Figure 2. Example POR operational diagram

It is important the user determines the timing (**Toff**) and threshold (**Voff**) levels by evaluating the performance in the specific system for which the device will be incorporated.

Software Reset via SPI

In order to guarantee proper reset regardless of **Voff** and **Toff**, a software reset can be issued via the SPI protocol. The SPI RESET command should be executed once Vdd reaches specified value.

The chip will ignore all SPI activity when nCS is held high, and the analog function will run. The analog function is powered down whenever nCS is low, but the SPI bus will function, allowing communication to enable and reset the KXR94/KXD94.

The sequence below describes how to use the SPI communication protocol to send the accelerometer the “Reset” command where the device will reboot the internal ASIC so the device power’s up with default RAM settings

Accelerometer SPI Reset Sequence

1. Power up KXR94/KXD94
2. Toggle nCS (Pin 9)
    a. nCS low to select
    b. nCS high for at least 200nS (SCLK = 5MHz)
    c. nCS low to select
3. Send Reset Command per Figure 3 (SDI is latched on rising edges of CLK) Note that it takes 16mSec for the Reset command to execute.

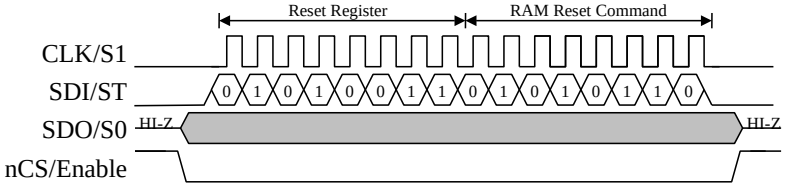

Figure 3. Reset Command Timing Diagram

4. Set nCS to high (Logic ‘1’) for Normal Analog Operation.

Application Diagram

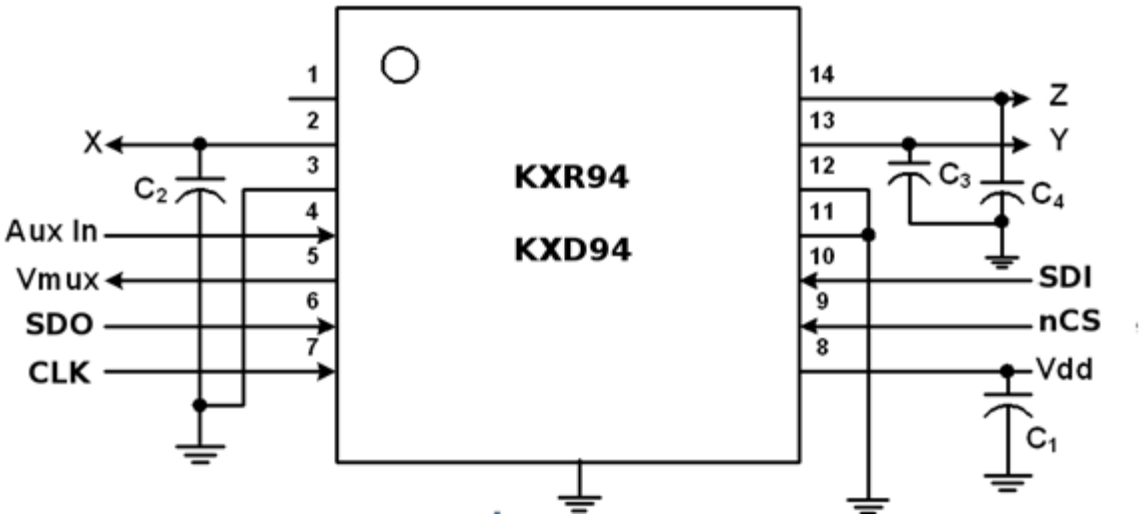

Figure 4. Application Diagram for KXR94 and KXD94 Reset