1. Introduction

This technical note is intended to provide information about the proper power-on procedure of the Kionix **KXTJ3,** and **KX003** accelerometers.

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD_{LOW}**, **T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{LOW}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the VDD ramp up time **T_{VDD}** be monotonic. To assure proper POR, the application should be evaluated over the customer specified range of **VDD, VDD_{LOW}**, **T_{VDD}, T_{VDD_OFF}** and temperature as POR performance can vary depending on these parameters

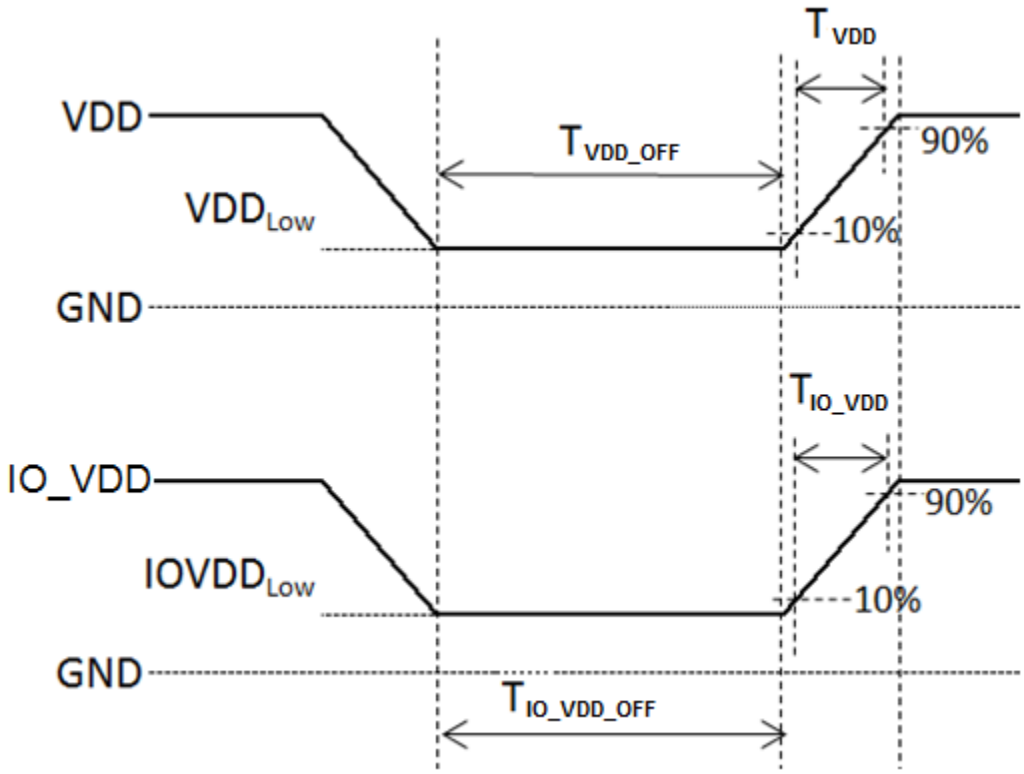

Figure 1: Power-On Reset Timing Diagram

36 Thornwood Drive, Ithaca, NY 14850 USA
Tel: 607-257-1080 — Fax: 607-257-1146
www.kionix.com — info@kionix.com

2. POR Performance

Bench Testing has demonstrated POR performance regions for a proper POR trigger. To assure POR trigger properly executes, setting operational thresholds consistent with Table 1 below is recommended.

Table 1: POR Performance

Parameters	Units	Min	Typical	Max
VDD rise time: T_{VDD}[1,2,3]	ms			5
IO_VDD rise time: T_{IO_VDD}[1,2,3]	ms			5
VDD off time: T_{VDD_OFF}[4,6]	ms	20		
IO_VDD off time: $T_{IO\_VDD\_OFF}$[4,6]	ms	20		
VDD low voltage: VDD_{Low}[4,6]	mV			200
IO_VDD low voltage: IO_VDD_{Low}[4,6]	mV			200
Software Reset Time[6]	ms			2
Power Up Time[7]	ms		12	30

Notes:

1. VDD and IO_VDD must always be monotonic ramps without ambiguous state
2. T_{VDD} and T_{IO_VDD} rise from 10% to 90% of final value needs to be ≤ 5 ms.
3. IO_VDD amplitude must remain ≤ VDD.
4. T_{VDD_OFF} and $T_{IO\_VDD\_OFF}$ are off times for VDD and IO_VDD rails respectively. To prevent the accelerometer from entering an ambiguous state, both VDD and IO_VDD need to be pulled down to GND (≤ 200mV) for duration of time ≥ 20 ms.
5. It is important the user determines the timing (**T_{VDD_OFF}**) and threshold (**VDD_{LOW}**) levels by evaluating the performance in the specific system for which the device will be incorporated.
6. Software Reset Time is defined as time it takes to perform a RAM reboot routine following the setting of SRST bit to 1 in the CTRL_REG2. The SRST bit will remain 1 until the RAM reboot routine is completed.
7. Power Up Time is defined as time from VDD and IO_VDD become valid to device boot completion.

3. Software Reset

Issuing the Software Reset command after the device was powered up is recommended. This is effective against dynamic or non-liner behavior of a power supply or unexpected noise above normal on the power rail during a power up.

3.1. I²C Interface

3.1.1. I²C Slave Addresses for Software Reset

The Software Reset command may need to be sent to **two** I²C slave addresses. The 7-bit slave address associated with the accelerometer is 00011YX, where the user programmable bit X, is determined by the assignment of ADDR (pin 1) to GND or IO_VDD. The factory programmable bit Y is set at the factory. An unsuccessful power-on may cause the internal value of the programmable bit Y to be flipped from 0 to 1 or 1 to 0. As a result, the user will need to take this into account and possibly send the required commands to the 'flipped' I²C address if attempts to send to the 'primary' address have failed. The Table 2 shows the 'primary' and 'flipped' 7-bit slave addresses for devices with ADDR pin connected to IO_VDD.

								Y	**X**
Description	**Address Pad**	**7-bit Address**	**<7>**	**<6>**	**<5>**	**<4>**	**<3>**	**<2>**	**<1>**
I²C Primary Address	IO_VDD	0x0F	0	0	0	1	1	**1**	1
I²C Flipped Address		0x0D	0	0	0	1	1	**0**	1

Table 2: I²C Slave Address #1 and #2 for Software Reset with ADDR pin at IO_VDD

The Table 3 shows the 'primary' and 'flipped' 7-bit slave addresses for devices with ADDR pin connected to GND.

								Y	**X**
Description	**Address Pad**	**7-bit Address**	**<7>**	**<6>**	**<5>**	**<4>**	**<3>**	**<2>**	**<1>**
I²C Primary Address	GND	0x0E	0	0	0	1	1	**1**	0
I²C Flipped Address		0x0C	0	0	0	1	1	**0**	0

Table 3: I²C Slave Address #1 and #2 for Software Reset with ADDR pin at GND

3.1.2. Software Reset Sequence following Power Up

a. Following the power up, write 0x00 to internal register 0x7F using I²C *Primary* Address as specified in Table 2 or Table 3 depending of the connection of ADDR pin. If command was acknowledged (ACK received), proceed to the next step while addressing the device using I²C *Primary* Address. If ACK was not received, resend the command using I²C *Flipped* Address. If command was acknowledged, proceed to the next step while addressing the device using I²C *Flipped* Address. If command was not acknowledged again, the device should be power cycled.

Register Name	Address		Value	
	Hex	Binary	Hex	Binary
0x7F	**0x7F**	**0111 1111**	**0x00**	**0000 0000**

b. Write 0x00 to Control Register 2 (CTRL_REG2). If NACK is received, the device should be power cycled.

Register Name	Address		Value	
	Hex	Binary	Hex	Binary
CTRL_REG2	**0x1D**	**0001 1101**	**0x00**	**0000 0000**

c. Write 0x80 to Control Register 2 (CTRL_REG2) to set the SRST bit to 1 to initiate software reset, which performs the RAM reboot routine. If software reset command was acknowledged (ACK received), wait for the duration of time specified in Table 1 for completion of the Software Reset and proceed to the next step. The SRST bit will also remain set to 1 until the RAM reboot routine is completed. If NACK is received, the device should be power cycled.

Register Name	Address		Value	
	Hex	Binary	Hex	Binary
CTRL_REG2	**0x1D**	**0001 1101**	**0x80**	**1000 0000**

d. Read content of "Who am I" register (WHO_AM_I) using the I²C *Primary* Address. The expected value is shown in Table 4 below. If value read is what is expected, proceed to the next step. If not, the software reset has failed and the device should be power cycled.

Part	Register Name	Address		Value	
		Hex	Binary	Hex	Binary
KXTJ3	**WHO_AM_I**	**0x0F**	**0000 1111**	**0x35**	**0011 0101**
KX003				**0x3F**	**0011 1111**

Table 4: Expected Value of Who_Am_I register

e. Read the content of DCST_RESP register. If read value is 0x55, the device operation can be started. If read value is not 0x55, the software reset has failed and the device should be power cycled.

Register Name	Address		Value	
	Hex	Binary	Hex	Binary
DCST_RESP	**0x0C**	**0000 1100**	**0x55**	**0101 0101**

3.1.3. Software Reset Timing Diagram

Figure 2 below shows an example of executing Software Reset sequence outlined in section 3.1.2 following a power up. The first attempt is to communicate with device using I²C *Primary* Address as specified in Table 2 or Table 3 depending of the connection of ADDR pin. If attempt is unsuccessful, the second attempt is to communicate with device using I²C *Flipped* Address mentioned in the same tables. Please wait for the duration of time specified in Table 1 for completion of the Software Reset before proceeding.

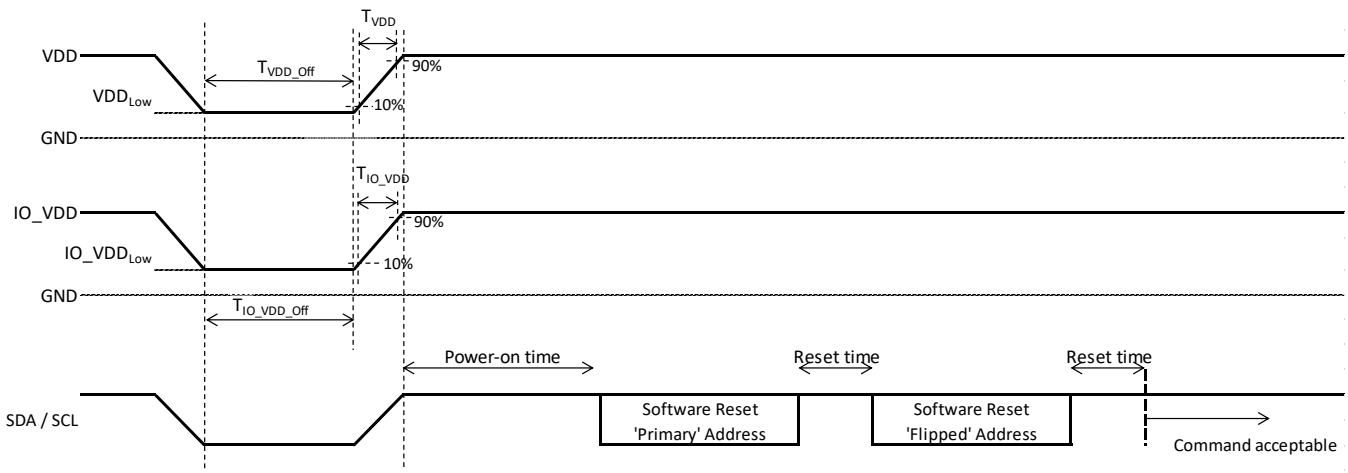

Figure 2: Power-On Timing Diagram followed by sending of two I²C Software Reset Commands