1. Introduction

The purpose of this application note is to help developers understand the design of the Advanced Data Path (ADP) available in select parts of the **KX13x** family (later to be referred as KX13x family) of tri-axial accelerometers and to provide guidance on how to configure the parameters for a typical application. Kionix strives to ensure that our accelerometers meet design expectations by default. However, every design has unique needs so default settings will not work in every environment. Depending on the intended application, it is very likely that some customization will be required to optimize performance. The information provided here will help the developer get the most out of these tri-axis accelerometers.

2. Application Schematic

This section shows recommended wiring for this accelerometer, based on proven operation of the part. Specific applications may require modifications from these recommendations. Please refer to the corresponding Product Specifications document for all pin descriptions.

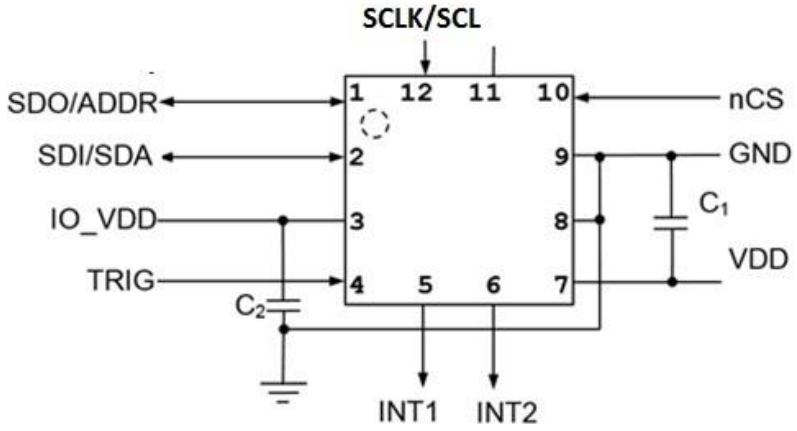

Figure 1: KX13x Family Application Schematic

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3. Design Overview

The **KX13x family** has two digital Data Paths - a Normal data path and an Advance data path, or ADP. Figure 2 and Figure 3 shows the block diagram in Low Power and High Performance modes respectively. Note that Advanced Data Path block is identical in either modes. The Advanced Data Path of the **KX13x family** consists of two configurable filters (filter-1, filter-2) and RMS calculation block. The first configurable filter (filter-1) is a 2nd order low-pass filter with an optional bypass. The second is another configurable filter (filter-2) that is configurable either as a low-pass or high-pass and an optional bypass. Both filter-1 and filter-2 can be configured as any type of filters such as Butterworth, Bessel or Chebyshev or even a custom filter. The data can be then routed to the RMS calculation block that has a configurable window size or bypass it. Lastly, the outputs from the Advanced Data Path can be routed to the dedicated output registers, Wake-up and/or Back-to-Sleep engines and the 512-byte FIFO buffer.

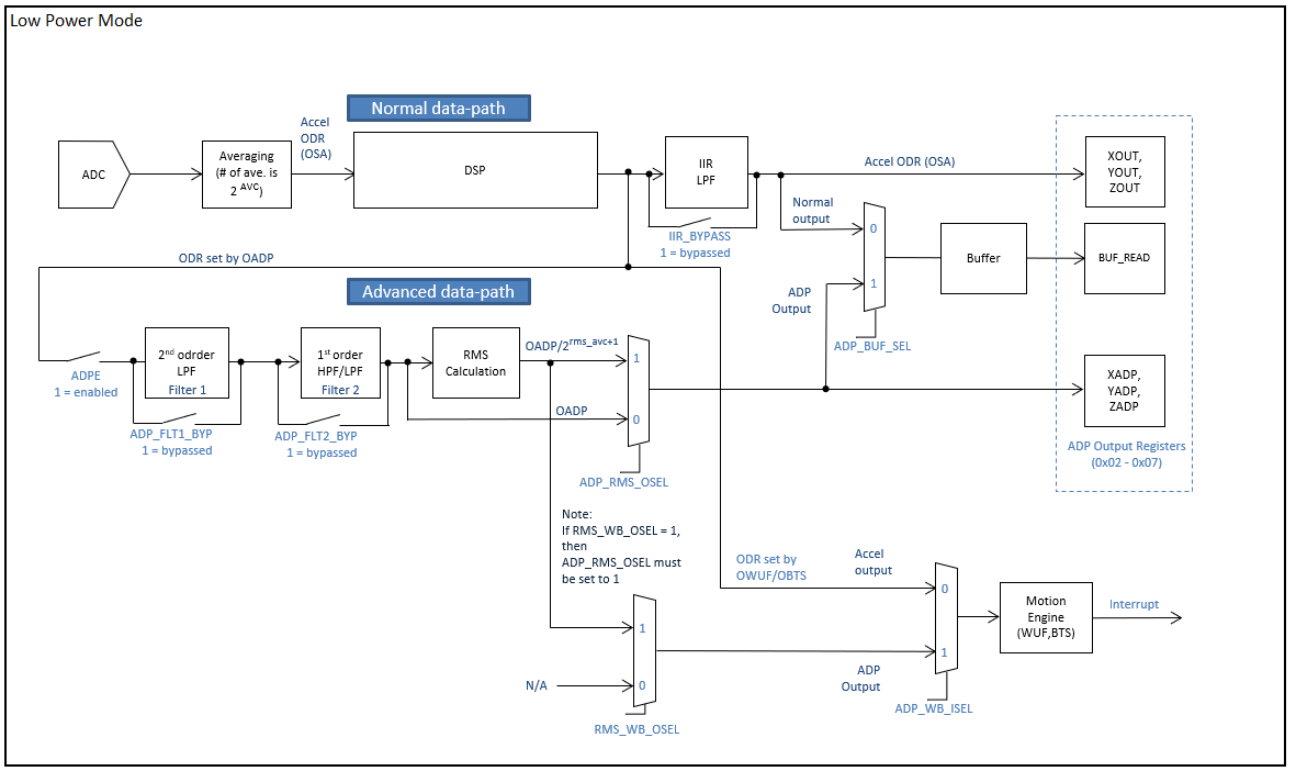


Figure 2: Normal and Advanced Data Paths of select KX13x accelerometers Operating in **Low Power Mode (RES=0)**

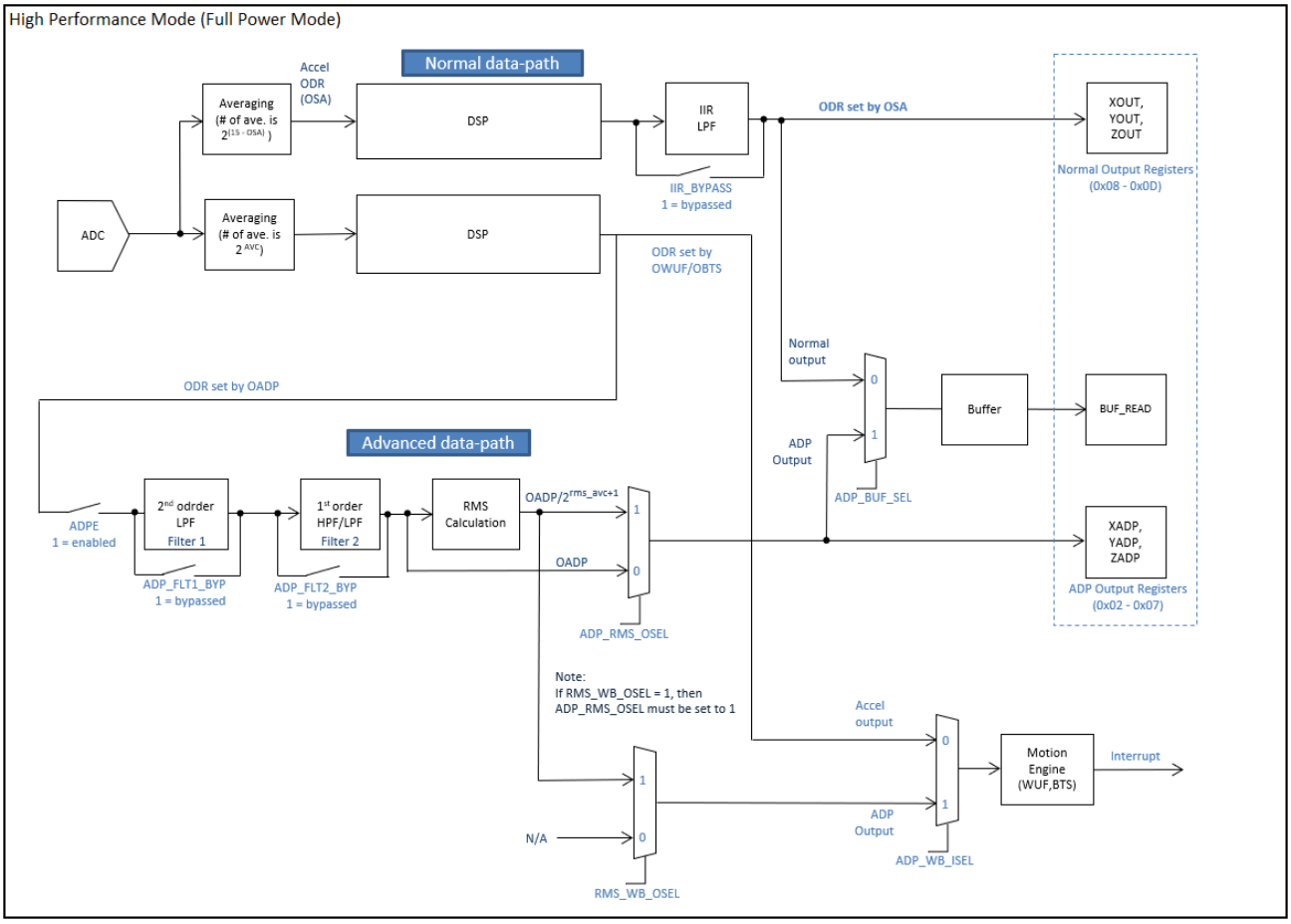


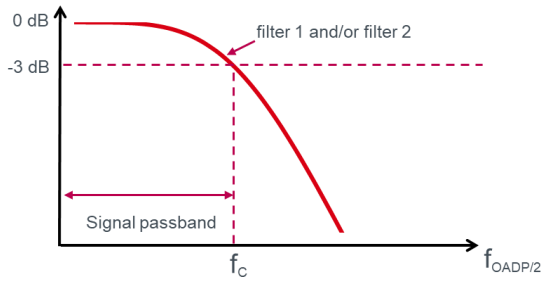
Figure 3: Normal and Advanced Data Paths of select KX13x accelerometers Operating in **High Performance Mode (RES=1)**

4. Options for ADP engine filtering modes

Possible use cases for filter-1 and filter-2 include configuration such as Low-pass, High-pass, Band-pass, and Band-reject filters. The RMS averaging stage can be utilized to assess how much energy is contained in the measured motion.

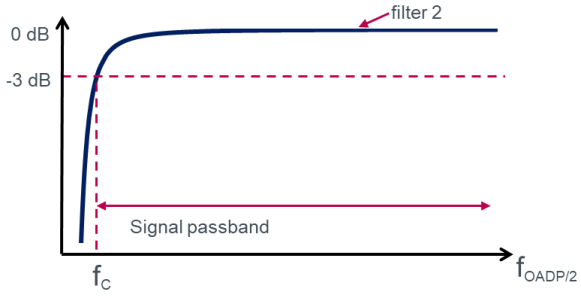
1. LP-filter mode

- By setting filter 1 and/or filter 2 as a low-pass filter, only signal components below the cut-off frequency f_C will be output.
- **Note 1:** filter 1 is 2nd order and filter 2 is 1st order, so they have different characteristics.
- **Note 2:** Both filter 1 and filter 2 can be used together for a steeper roll-off curve.



2. HP-filter mode

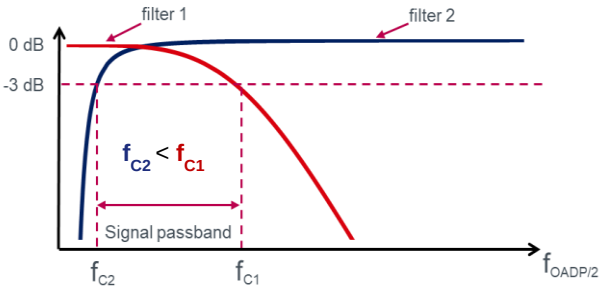
- Only filter 2 can be applied as a high-pass filter, where only signal above cut-off frequency f_C will be output.
- **Note:** filter 1 should be bypassed.
- If RMS calculation engine is used, high-pass filtering will remove the gravity offset



3. Band-pass filter mode

- f_{C1} and f_{C2} are the cut-off frequencies of the low-pass and high-pass filters.
- Signal is passed between f_{C1} and f_{C2} with *attenuation = product of the magnitude responses of two filters*

  e.g. (-1.5 dB) + (- 0.75 dB) = -2.25 dB.
- The distance between f_{C1} and f_{C2} should be optimized case by case to fit your own needs.



5. Quick Start Implementations

Here we present options to initialize the Advanced Data Path based on desired behavior. The register settings below are meant as starting points, which will need to be expanded upon for most specific use cases. Please refer to the Product Specification / Technical Reference Manual for more details on register bits, functionality, and general sensor operation.

5.1. Band Pass Filter Example

This example configures and enables the accelerometer to use the Advanced Data Path as a Band Pass Filter for 200Hz-400Hz with the RMS engine enabled. This is accomplished by setting filter-1 to low pass below 400Hz, and filter-2 to high pass above 200Hz at a data rate of 1600Hz.

- Write 0x00 to Control 1 (CNTL1) to set the accelerometer in stand-by mode

Register Name	Address	Value
CNTL1	0x1B	0x00

- Write 0x10 to Control 5 (CNTL5) to enable the Advanced Data Path

Register Name	Address	Value
CNTL5	0x1F	0x10

- Write 0x8B to Output Data Control Register (ODCNTL) to bypass the IIR Filter, set IIR filter corner frequency to ODR/9 (default), disable Fast Start, and set the ODR to 1600Hz.

Register Name	Address	Value
ODCNTL	0x21	0x8B

- Write 0x73 to Low Power Control Register 1 (LP_CNTL1) to set a 128-sample average for optimizing current and noise performance.

Register Name	Address	Value
LP_CNTL1	0x3A	0x73

- Write 0x3B to Advanced Data Path Control Register 1 (ADP_CNTL1) to set the number of samples used to calculate RMS output to 16, and to set Advanced Data Path ODR to 1600Hz.

Register Name	Address	Value
ADP_CNTL1	0x64	0x3B

- Write 0x03 to Advanced Data Path Control Register 2 (ADP_CNTL2) to make sure Filter 1 and Filter 2 are not bypassed, to select the RMS data out to XADP, YADP, and ZADP registers, and to set Filter-2 as a High-pass filter.

Register Name	Address	Value
ADP_CNTL2	0x65	0x03

- Write 0x16 to Advanced Data Path Control Register 3 (ADP_CNTL3) to set Filter-1 Coefficient $(1/A)$ to pass only data below 400Hz. *See Table 1,* row $SR/4$ to set Filter-1 LPF $fc = 400Hz$ with $SR = 1600Hz$. $adp\_f1\_1a = 22\ (dec) = 16\ (hex)$.

Register Name	Address	Value
ADP_CNTL3	0x66	0x16

- Write 0x00 to Advanced Data Path Control Register 4 (ADP_CNTL4), Advanced Data Path Control Register 5 (ADP_CNTL5), and Advanced Data Path Control Register 6 (ADP_CNTL6) to set Filter-1 Coefficient (B/A) to pass only data below 400Hz. *This step is optional as this is also a default setting.* See Table 1, row $SR/4$ to set Filter-1 LPF $fc = 400Hz$ with $SR = 1600Hz$. $adp\_f1\_ba = 0\ (dec) = 00\ (hex)$.

Register Name	Address	Value
ADP_CNTL4	0x67	0x00
ADP_CNTL5	0x68	0x00
ADP_CNTL6	0x69	0x00

- Write 0x1A to Advanced Data Path Control Register 7 (ADP_CNTL7), 0xF6 to Advanced Data Path Control Register 8 (ADP_CNTL8), and 0x15 to Advanced Data Path Control Register 9 (ADP_CNTL9) to set Filter-1 Coefficient (C/A). *See Table 1,* row $SR/4$ to set Filter-1 LPF $fc = 400Hz$ with $SR = 1600Hz$. $adp\_f1\_ca = 1439258\ (dec) = 15F61A\ (hex)$.

Register Name	Address	Value
ADP_CNTL7	0x6A	0x1A
ADP_CNTL8	0x6B	0xF6
ADP_CNTL9	0x6C	0x15

- Write 0x01 to Advanced Data Path Control Register 10 (ADP_CNTL10) to set ADP shift scale value for Filter-1. *See Table 1,* row $SR/4$ to set Filter-1 LPF $fc = 400Hz$ with $SR = 1600Hz$. $adp\_f1\_ish = 1\ (dec) = 01\ (hex)$.

Register Name	Address	Value
ADP_CNTL10	0x6D	0x01

- Write 0xB5 to Advanced Data Path Control Register 11 (ADP_CNTL11). This register consists of adp_fi_osh (1bit) and adp_f2_1a (7bit). *See Table 1,* row $SR/4$ to set Filter-1 LPF $fc = 400Hz$ with $SR = 1600Hz$. $adp\_f1\_0sh = 1\ (dec)$. *See Table 3,* row $SR/8$ to set Filter-2 HPF $fc = 200Hz$ with $SR = 1600Hz$. $adp\_f2\_1a = 53\ (dec)$.

Register Name	Address	Value
ADP_CNTL11	0x6E	0xB5

- Write 0x05 to Advanced Data Path Control Register 12 (ADP_CNTL12), 0x35 to Advanced Data Path Control Register 13 (ADP_CNTL13) to set Filter-2 coefficient (B/A). *See Table 3,* row $SR/8$ to set Filter-2 HPF $fc = 200Hz$ with $SR = 1600Hz$. $adp\_f2\_ba = 13573\ (dec) = 3505\ (hex)$.

Register Name	Address	Value
ADP_CNTL12	0x6F	0x05
ADP_CNTL13	0x70	0x35

- Write 0x02 to Advanced Data Path Control Register 18 (ADP_CNTL18), to set ADP input scale shift value for Filter-2. *See Table 3,* row $SR/8$ to set Filter-2 HPF $fc = 200Hz$ with $SR = 1600Hz$. $adp\_f2\_ish = 2\ (dec) = 02\ (hex)$.

Register Name	Address	Value
ADP_CNTL18	0x75	0x02

- Write 0x02 to Advanced Data Path Control Register 19 (ADP_CNTL19), to set ADP output scale shift value for Filter-2. *See Table 3,* row $SR/8$ to set Filter-2 HPF $fc = 200Hz$ with $SR = 1600Hz$. $adp\_f2\_0sh = 2\ (dec) = 02\ (hex)$.

Register Name	Address	Value
ADP_CNTL19	0x76	0x02

- Write 0x20 to Interrupt Control Register 1 (INC1) to enable the physical interrupt pin in active-low mode, latching until cleared by reading INT_REL.

Register Name	Address	Value
INC1	0x22	0x20

- Write 0x10 to Interrupt Control Register 4 (INC4) to set the Data ready interrupt to report on physical interrupt pin INT1.

Register Name	Address	Value
INC4	0x25	0x10

- Write 0xB0 to Control 1 (CNTL1) to set the accelerometer into operating mode (PC1=1), low power mode (RES=0), data ready enabled (DRDYE=1) and the third g-range of the full-scale available on the part (GSEL<1:0> = 0x02).

Register Name	Address	Value
CNTL1	0x1B	0xB0

- Band Pass RMS acceleration data can now be read from the XADP_L, XADP_H, YADP_L, YADP_H, ZADP_L, and ZADP_H registers in 2's complement format synchronously. To reduce duplicate sensor data, wait at least 1/ODR period before reading the next sample.

6. Appendix

6.1. Example of Coefficients

The ADP_CNTL3 to ADP_CNTL19 registers defines A, B and C coefficients.

Note: In the examples below, SR (Sampling Rate) refers to the Advanced Data Path Output Data Rate as set by OADP<3:0> bits in ADP_CNTL1 register. Target cutoff, f_C, is the only variable that scales with SR. Other coefficients remain the same at different ODRs. So (as in the example 5.1) if SR = 1600 Hz instead of 25600 Hz, then SR/4 = 400 = f_C in row one, with the same coefficients of 1/A = $2.9E^{-01}$, B/A = $1.3E^{-16}$, C/A = $1.7E^{-01}$. Compare the register settings from example 5.1 against row one of the tables below to verify.

Visit our online Advanced Datapath Simulation Tool to view examples of ADP outputs for different settings.

6.1.1. Filter-1 – Low-Pass (SR = 25600Hz, K_0 = 1)

Sampling Rate Ratio	target cut-off fc [Hz]	Sensor register bits				
		rms_f1_1a	rms_f1_ba	rms_f1_ca	rms_f1_ish	rms_f1_osh
SR/4	6400	22	0	1439258	1	1
SR/8	3200	72	3954428	2796203	2	0
SR/16	1600	117	6099540	4815580	4	0
SR/32	800	10	7230041	6354764	5	0
SR/64	400	20	7807115	7301172	7	0
SR/128	200	25	8097550	7826024	9	0
SR/256	100	27	8243038	8102435	11	0
SR/512	50	29	8315818	8244280	13	0
SR/1024	25	29	8352212	8316131	15	0
SR/2048	12.5	30	8370410	8352291	17	0

Table 1: Example of Filter-1 Coefficients

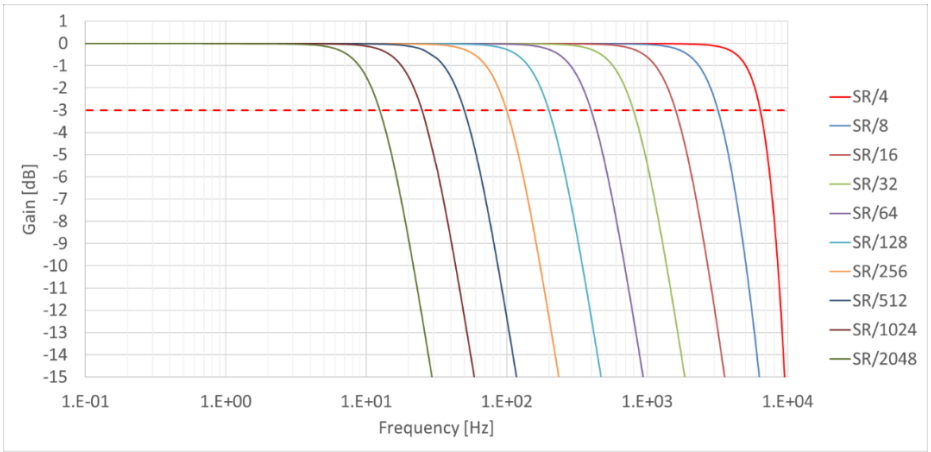


Figure 4: Example of Filter-1 Magnitude Response

6.1.2. Filter-2 – Low-Pass (SR = 25600Hz, K_0 = 1)

Sampling Rate Ratio	target cut-off fc [Hz]	Sensor register bits			
		rms_f2_1a	rms_f2_ba	rms_f2_ish	rms_f2_osh
SR/4	6400	0	0	1	1
SR/8	3200	22	13573	1	0
SR/16	1600	42	21895	2	0
SR/32	800	56	26892	3	0
SR/64	400	64	29699	4	0
SR/128	200	68	31198	5	0
SR/256	100	71	31973	6	0
SR/512	50	72	32368	7	0
SR/1024	25	72	32568	8	0
SR/2048	12.5	73	32668	9	0

Table 2: Example of Filter-2 (Low-Pass) Coefficients

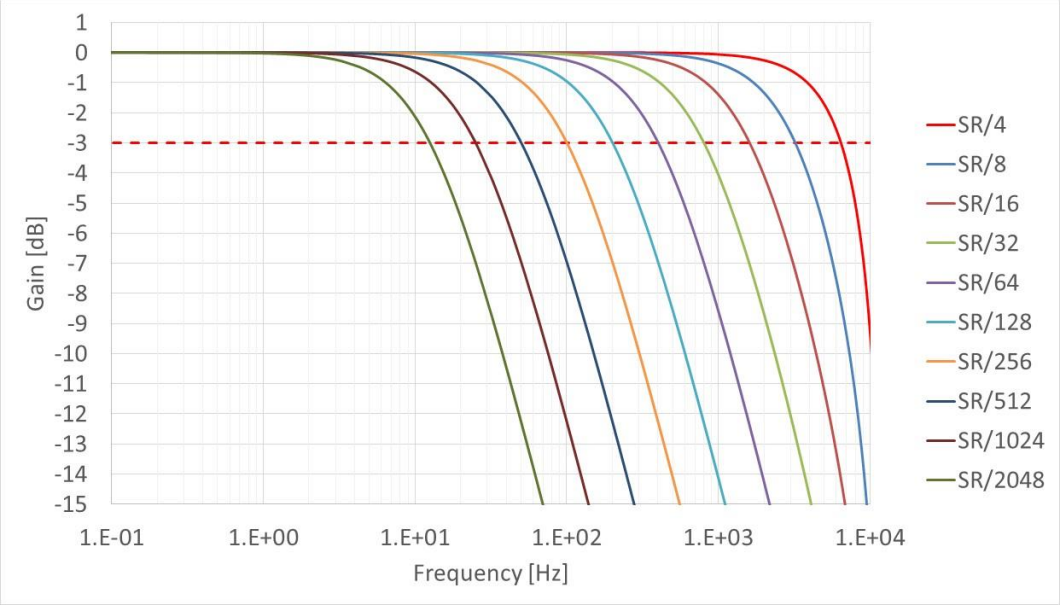


Figure 5: Example of Filter-2 (Low-Pass) Magnitude Response

6.1.3. Filter-2 – High-Pass (SR = 25600Hz, K_0 = 1)

Sampling Rate Ratio	target cut-off fc [Hz]	ASIC register bits			
		rms_f2_1a	rms_f2_ba	rms_f2_ish	rms_f2osh
SR/4	6400	0	0	1	1
SR/8	3200	53	13573	2	2
SR/16	1600	86	21895	3	3
SR/32	800	105	26892	4	4
SR/64	400	116	29699	5	5
SR/128	200	122	31198	6	6
SR/256	100	125	31973	7	7
SR/512	50	126	32368	8	8
SR/1024	25	127	32568	9	9
SR/2048	12.5	0	32668	9	10

Table 3: Example of Filter-2 (High-Pass) Coefficients

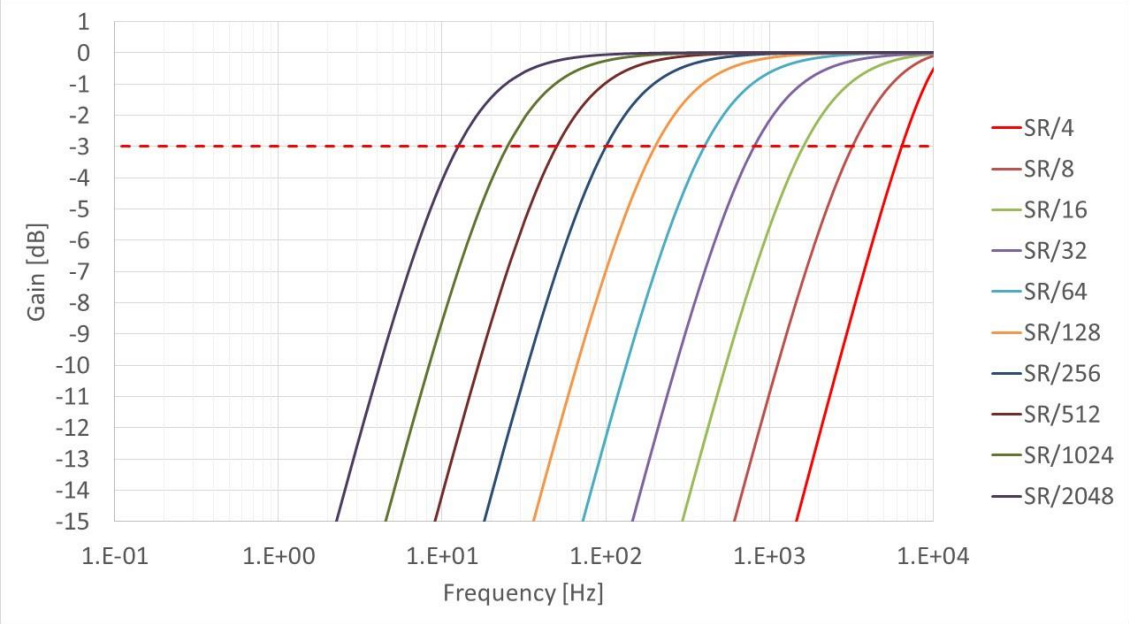


Figure 6: Example of Filter-2 (High-Pass) Magnitude Response